

NPTEL » Computer architecture and organization

Announcements

About the Course

Ask a Question

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How does an NPTEL online course work? Week 0		
Computer Systems		
Lecture 2: Basic Operation A Computer	n of	
Lecture 3: Memory Addressing and Language	es	
Lecture 4: Software and Architecture Types		
Lecture 5: Instruction Set Architecture		
Week 1 Lecture Material		
Week 1 Practice Problems	S	
Quiz: Week 1 : Assignment	ent	
Feedback Form for Week	1	

Thank you for taking the Week 1: Assignment 1.

Week 1: Assignment 1

Your last recorded submission was on 2021-08-14, 23:32 IST

Which of the following is/are false?

1 point

1 point

Due date: 2021-08-18, 23:59 IST.

- a. Processor can directly access data from secondary memory.
- b. Primary memory are used as backup memory.
- Primary memory stores the active instructions and data for the program being executed on the processor.
- d. Primary memory can store only instructions.
- a.
- ✓ b.
- □ c.
- d.
- 2) Program counter:
 - a. Counts the total number of instructions present in a program.
 - b. Points to the current instruction that is being executed.
 - Points to the next instruction that is to be executed.
 - d. Stores the data of the current instruction that is being executed.
- a.
- b.
- O
- \bigcirc d.

Week 4	Which of the following is/are false?	1 point
DOWNLOAD VIDEOS	 a. Central Processing Unit (CPU) consists of Control Unit, Arithmetic Logic Unit (ALU) and Primary Memory. b. There are broadly two types of memory, primary memory and secondary memory. c. The arithmetic and logic operations are performed in the control unit. d. Control Unit is a part of main memory. 	
	 ☑ a. ☑ b. ☑ c. ☑ d. Which of the following contains circuitry to carry out operations such as addition, multiplication etc? 	1 point
	a. Control Unit b. Memory Unit c. Input/output Unit d. None of these.	
	 ○ a. ○ b. ○ c. ● d. 	

- Tow registers are initialized as R1=30 and R2 = 25. The instruction ADD R1, R2 is in memory location 2018H. If the size of an instruction is 4 byte, then after the execution of the instruction the value of PC, R1 and R2 will be.
 - a. PC = 2018H, R1 = 55, R2 = 25
 - b. PC = 2018H, R1 = 55, R2 = 00
 - c. PC = 201CH, R1 = 55, R2 = 00
 - d. PC = 201CH, R1 = 55, R2 = 25
- a.
- Ob.
- O c.
- d.
- Consider a 32-bit machine where an instruction (SUB R1, LOCA) is stored at location 2004H.

 LOCA is a memory location whose value is 1024H. The number of memory access required to execute this instruction will be?

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- Consider a 32-bit machine where an instruction (ADD R1, R2) is stored at memory location 2004H (in hexadecimal). What will be the value of IR and PC while the instruction is fetched and executed? Consider Individual instruction is 32-bit.
 - a. IR = ADD R1, R2, PC = 2004H
 - b. IR = 2004H, PC = ADD R1, R2
 - c. IR = ADD R1, R2, PC = 2008H
 - d. IR = 2008H, PC = ADD R1, R2
 - a.
 - Ob.
 - C.
 - \bigcirc d.

1 point

1 point

1 point

8)	For a 512 X 32 bit memory that contains 512 locations each with 32-bit data, what will be the address (in binary) of the 389 th location? (Assume first location as 0)	1 point
	a. 110000100 b. 110000101 c. 011000100 d. 011000101	
(● a.○ b.○ c.○ d.	
9)	Consider the instruction XOR R3, R2. If register R1 and R2 contains value 09H and 47H respectively. What will be the value R3 after executing the instruction? a. 4E b. 2E c. 3E d. 5E	1 point
	 a. b. c. d. e. 	
10)	For a byte addressable computer which has 4Gigabytes of memory. If each word in the computer is 64bit. Then how many bits are needed to address a single word.	1 point
	a. 29 b. 30 c. 31 d. 32	
(a.b.c.d.	

11)	Consider the following statement and answer:	1 point
	(i) In Von-Neumann architecture, instruction and data are stored in same memory modu	e.
	(ii) In Von-Neumann architecture, instruction and data access can be performed parallell	y.
	a. Only (i) is true.	
	b. Only (ii) is true.	
	c. Both (i) and (ii) are true.	
	d. Both (i) and (ii) are false.	
	a.	
	D b. D c.	
	D d.	
40)		
12)	Which of the following statement(s) is/are true?	1 point
	a. Nibble: A collection of 4 bits	
	b. Word: Byte/Multiple of Bytes	
	c. Byte: A collection of 8-bit	
	d. All of these	
) a.	
	D b. D c.	
	d .	
	nay submit any number of times before the due date. The final submission will be considered for grading.	